WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a plurality of memory cells, arranged in rows and columns, each including a latch circuit formed of insulated gate type field effect transistors of first and second conductivity types each having a back gate; and

substrate potential changing circuitry for changing a back gate potential of at least the insulated gate type field effect transistor of the first conductivity type of a selected memory cell in a data writing from said back gate potential in a data reading in response to an address signal and an operation mode designating signal.

2. The semiconductor memory device according to claim 1, wherein

said insulated gate type field effect transistor of the first conductivity type is a P channel insulated gate type field effect transistor, and

said substrate potential changing circuitry sets the back gate potential of the P channel insulated gate type field effect transistor of said selected memory cell in said data writing to a voltage level higher than in said data reading.

3. The semiconductor memory device according to claim 2, wherein said substrate potential changing circuitry sets the back gate potential of said P channel insulated gate type field effect transistor to an external interfacing power supply voltage level in said data writing.

4. The semiconductor memory device according to claim 2, wherein

each of the memory cells receives a power source voltage as a power supply voltage for high level data storage, and

said substrate potential changing circuitry sets the back gate potential of said P channel insulated gate type field effect transistor to said power source voltage level in

said data writing and to a voltage level lower than said power source voltage in said data reading.

5. The semiconductor memory device according to claim 1, wherein

said substrate potential changing circuitry includes

a plurality of substrate voltage transmission lines, arranged corresponding to the respective memory cell columns, each coupled commonly to the back gates of the insulated gate type field effect transistors of the first conductivity type in a corresponding column, and

a plurality of substrate potential setting circuits, arranged corresponding to the respective columns, each for setting a voltage of a corresponding substrate voltage transmission line in response to said operation mode designating signal and a column select signal generated based on said address signal.

6. The semiconductor memory device according to claim 5, wherein

said insulated gate type field effect transistor of the first conductivity type is a P channel insulated gate type field effect transistor, and

said substrate potential changing circuitry makes a back gate potential of the P channel insulated gate type field effect transistor in a selected column higher than in the memory cell on a non-selected column when said operation mode designating signal designates the data writing.

7. The semiconductor memory device according to claim 1, wherein

said insulated gate type field effect transistor of the first conductivity type is an N channel insulated gate type field effect transistor, and

said substrate potential changing circuitry makes a back gate potential of the N channel insulated gate type field effect transistors lower than in the data reading when said operation mode designating signal designates the data writing.

8. The semiconductor memory device according to claim 7, wherein said substrate potential changing circuitry sets the back gate potential of said N type insulated gate type field effect transistor to a ground voltage level in said data writing.

9. The semiconductor memory device according to claim 7, wherein

each of the memory cells receives a ground voltage as a power supply voltage for low level data storage, and

said substrate potential changing circuitry sets the back gate potential of said N channel insulated gate type field effect transistor to a voltage level higher than said ground voltage in said data writing and to said ground voltage level in said data reading.

10. The semiconductor memory device according to claim 1, wherein

said substrate potential changing circuitry includes

a plurality of first substrate voltage transmission lines, arranged corresponding to the respective memory cell columns, each commonly coupled to the back gates of the insulated gate type field effect transistors of the first conductivity type of the memory cells on a corresponding column,

a plurality of second substrate voltage transmission lines, arranged corresponding to the respective columns, each commonly coupled to the back gates of the insulated gate type field effect transistors of the second conductivity type of the memory cells on the corresponding column, and

a plurality of substrate potential selecting circuits, arranged corresponding to the respective columns, each for setting voltages of corresponding first and second substrate voltage transmission lines in response to said operation mode designating signal and a column select signal generated based on said address signal.

11. The semiconductor memory device according to claim 10, wherein said substrate potential changing circuitry makes back gate potentials of the insulated gate

type field effect transistors of the first conductivity type in a selected column higher while making back gate potentials of the insulated gate type field effect transistors of the second conductivity type lower when said operation mode designating signal designates data reading.

12. The semiconductor memory device according to claim 1, wherein

said substrate potential changing circuitry includes

a plurality of substrate voltage transmission lines, arranged corresponding to the respective memory cell columns, each for transmitting a bias voltage to the back gates of the insulated gate type field effect transistors of the first conductivity type of the memory cells on a corresponding column,

a plurality of substrate potential setting circuits, arranged corresponding to the respective memory cell columns, each for setting a potential of the substrate voltage transmission line in a corresponding column in accordance with said operation mode designating signal and said column select signal generated based on the address signal, and

a substrate potential auxiliary circuit for driving the potential of the substrate voltage transmission line on the selected column toward a prescribed potential for a prescribed time period in response to said operation mode designating signal and said column select signal.

13. The semiconductor memory device according to claim 1, wherein

the insulated gate type field effect transistor of the first conductivity type of the memory cell is formed in a first substrate region, and the insulated gate type field effect transistor of the second conductivity type of said memory cell is formed in a second substrate region,

the first and second substrate regions are each formed, continuously in a column direction, corresponding to each column, and form the back gates of the

insulated gate type field effect transistors of the first and second conductivity type, respectively, of the memory cells arranged in a corresponding column, and

said substrate potential changing circuitry changes a potential of at least one of said first and second substrate regions.

14. The semiconductor memory device according to claim 13, further comprising a power line extending continuously in a column direction and commonly coupled to the insulated gate type field effect transistors of the first conductivity type of the memory cells arranged in alignment in the column direction.

15. The semiconductor memory device according to claim 13, wherein said first and second substrate regions are formed on an insulating film, and said first and second substrate regions are isolated by a trench region.

16. The semiconductor memory device according to claim 15, wherein said first and second substrate regions are isolated in units of columns.

17. The semiconductor memory device according to claim 1, wherein said substrate potential changing circuitry changes a potential application manner of the back gates for said plurality of memory cells between a standby state, said data reading and said data writing, in response to said operation mode designating signal.